DIFFERENTIAL SAMPLING CIRCUIT FOR GENERATING A DIFFERENTIAL INPUT SIGNAL DC OFFSET

ABSTRACT OF THE DISCLOSURE

A differential sampling circuit is configured around a differential operational amplifier and is provided with a pair of switched-capacitor networks, each including an circuit block, to generate the real value of the differential input signal DC offset at each system clock cycle. During the first half cycle, the differential input signal pair (Vin+,Vin-) is sampled and the holding capacitors in each network are charged. During the second half cycle, the differential input signal pair is sampled again and the holding capacitors are further charged. At the end of the cycle, the charges held in the holding capacitors are applied to the differential operational amplifier, so that the differential output signal is equal to the real differential input signal DC offset value.